AMENDMENTS TO THE CLAIMS

The following is a complete listing of the claims indicating the current status of each claim:

1-40 (canceled)

41. (new) A high-performance apparatus for data conversion, comprising:

a. a conversion unit that includes at least two lower-performance converters, each said converter having at least one lower performance parameter than the high-performance apparatus for data conversion, said conversion unit operative to convert an input signal obtained in a time domain;

b. a processing unit coupled to said conversion unit and operative to process frequency domain information extracted from said input signal, and, based on said processed frequency domain information, operative to provide in combination with said conversion unit at least two processed signals; and

c. a recombining unit operative to combine said at least two processed signals into a single high-performance output signal.

42. (new) The apparatus of claim 41, wherein said processing unit includes:

i. a transform unit operative to perform on said input signal a transform from said time domain to a frequency domain to provide a frequency domain input signal,

ii. a frequency domain information extraction unit operative to perform said extraction through a division of said frequency domain into at least two frequency domain parts, one said part related to a low-resolution signal to noise ratio (SNR) and the other said part related to a high-resolution SNR, and

iii. a processor operative to process said frequency domain information.

43. (new) The apparatus of claim 42, wherein each of said at least two lower performance converters is an analog-to-digital converter, wherein said input signal is an analog input signal, wherein one of said at least two processed signals is a first processed digital signal jointly processed by a first of said analog-to-digital converters (ADC1) and by said processing unit, and wherein a second of said processed signals is a second

processed digital signal jointly processed by a second of said analog-to-digital converters (ADC2) and by said processing unit.

44. (new) The apparatus of claim 43, further comprising

d. a subtractor operative to subtract an analog subtraction signal processed by said processor from said analog input signal, said subtractor providing an analog error signal that is further converted by said ADC2 into an ADC2 output signal.

45. (new) The apparatus of claim 44, wherein said transform unit includes a digital transform unit operative to perform said transform and to provide said frequency domain input signal, wherein said frequency domain information extraction unit includes a spectral analysis unit operative to perform said division of said frequency domain into at least an upper frequency domain part and a lower frequency domain part by identifying said upper frequency domain part with a threshold, and wherein said processor includes:

A. a digital filtering unit operative to perform digital filtering of frequencies below said threshold and to provide a first digitally filtered output,

B. an inverse transform function operative to inversely transform said first digitally filtered output back into a first filtered time domain digital signal, and

C. a first digital-to-analog converter (DAC1) operative to convert said first filtered time domain digital signal into said analog subtraction signal.

46. (new) The apparatus of claim 44, further comprising:

e. a calibration/equalization unit operative to calibrate the apparatus.

47. (new) The apparatus of claim 46, wherein said calibration/equalization unit is operating in the digital frequency domain

48. (new) The apparatus of claim 46, wherein said processor further includes a post-DAC filtering unit operative to filter an analog subtraction signal prior to its input to said subtractor, whereby said post-DAC filtering provides a further improvement in the high-performance of the apparatus.

49. (new) The apparatus of claim 44, wherein said transform unit includes a digital transform unit operative to perform said transform and to provide said frequency domain input signal, wherein said frequency domain information extraction unit includes a spectral

analysis unit operative to perform said division of said frequency domain into at least an upper frequency domain part and a lower frequency domain part by identifying said upper frequency domain part with a threshold, and wherein said processor includes:

A. a digital filtering unit operative to perform digital filtering of frequencies below said threshold and to provide a first digitally filtered output,

B. an inverse transform function operative to inversely transform said first digitally filtered output back into a first filtered time domain digital signal, and

C. a subtraction signal synthesizer operative to synthesize said analog subtraction signal from frequency domain information.

50. (new) The apparatus of claim 46, wherein said transform unit includes a first Fast Fourier Transform (FFT1) function operative to perform said transform and provide said frequency domain input signal, wherein said frequency domain information extraction unit includes a spectral analysis unit operative to perform said division of said frequency domain into at least an upper frequency domain part and a lower frequency domain part by identifying said upper frequency domain part with a threshold, and wherein said processor includes:

A. a first spectral window filter operative to perform digital filtering of frequencies below said threshold and to provide a first digitally filtered output,

B. a first inverse Fast Fourier Transform (IFFT1) function operative to inversely transform said first digitally filtered output back into a first filtered time domain digital signal, and

C. a first digital-to-analog converter (DAC1) operative to convert said first filtered time domain digital signal to provide said analog subtraction signal.

51. (new) The apparatus of claim 50, further comprising:

e. a second Fast Fourier Transform (FFT2) function operative to perform a transform from the time domain to the frequency domain on said ADC2 output signal to provide an FFT2 output signal;

f. a second spectral window filter operative to perform digital filtering of frequencies above said threshold and to provide a second digitally filtered output

g. a digital summer for recombining said first and second digitally filtered outputs and for providing an FFT sum output, and

h. a second inverse Fast Fourier Transform (IFFT2) function operative to inversely transform said FFT sum output into a second filtered time domain digital signal.

52. (new) The apparatus of claim 51, wherein said recombining unit includes a digital spectral combining unit operative to provide an optional frequency domain digital output and a transform-to-time unit operative to provide a time domain digital output.

53. (new) A high-resolution, high-speed apparatus for data conversion, comprising:

a a first, low-resolution analog-to-digital converter (ADC1) operative to output a first digital output signal in a time domain;

b. a first spectral signal processor operative to use a frequency domain to both convert said first digital output signal into an output analog subtraction signal and to provide a processed digital signal;

c. a second low-resolution analog-to-digital converter (ADC2) operative to convert an analog error signal formed in a subtraction operation involving said output analog subtraction signal into a second digital output signal; and

d. a digital combining unit operative to receive said processed digital signal and said second digital output signal and to combine both said signals into a final digital output signal;

whereby the apparatus has a higher resolution that either said ADC1 or said ADC1, and

whereby the data conversion is performed in the frequency domain using spectral tools, thereby providing an improved dynamic range and quantization noise, a reduction or elimination of critical analog circuit requirements and bottlenecks, and an increase of the sampling rate relative to existing pipeline/subranging architectures.

54. (new) The apparatus of claim 53, further comprising:

e. a splitter connected to said ADC1 and operative to split an input analog signal into a main channel analog signal used in said subtraction operation and a secondary subtraction channel analog signal input to said ADC1, said main channel analog signal fed to said ADC1.

55. (new) The apparatus of claim 54, further comprising:

f. a subtractor operative to perform said subtraction operation; and

g. a delay inserted in a path between said splitter and said subtractor and operative to compensate for delays occurring in said subtraction channel.

56. (new) The apparatus of claim 53, wherein said digital combining unit includes a digital spectral combining unit operative to provide an optional frequency domain digital output, and a transform-to-time unit operative to provide a time domain digital output.

57. (new) The apparatus of claim 55, further comprising:

h. an amplitude scaling unit coupled to said ADC2 and operative to adapt said analog error signal to a range of said ADC2;

i. a separate optional digital combining unit operative to combine said first and second digital output signals of respectively said ADC1 and ADC2 and to output an optional digital signal; and

j. at least one optional second spectral signal processor coupled to said ADC2 and to said digital combining unit and operative to provide at least one additional subtraction stage.

58. (new) The apparatus of claim 53, wherein said first spectral signal processor includes:

i. a transform function operative to transform said first digital output signal from said time domain to said frequency domain, thereby providing a first transformed digital signal;

ii. a spectral analysis unit operative to perform spectral analysis in said frequency domain using said first transformed digital signal and to provide output frequency information that includes a dynamic frequency range divided into above-threshold frequencies and below-threshold frequencies;

iii. a digital filtering unit operative to strongly attenuate said below-threshold frequencies and to transfer without attenuation said above-threshold frequencies to provide a digitally filtered output;

iv. an inverse transform function operative to inversely transform said digitally filtered output into an inversely transformed output; and

v. a first digital-to-analog converter (DAC1) operative to receive and convert said output frequency information and said inversely transformed output into said output analog subtraction signal.

59. (new) The apparatus of claim 58, wherein said first spectral signal processor further includes a post-DAC analog filtering unit coupled to said subtractor and operative to filter said output analog subtraction signal prior to its input to said subtractor.

60. (new) The apparatus of claim 58, wherein said transform function is performed by a Fast Fourier Transform (FFT) and wherein said inverse transform function is performed by an Inverse Fast Fourier Transform (IFFT).

61. (new) The apparatus of claim 58, wherein said transform function is performed by a filter bank.

62. (new) The apparatus of claim 53, wherein said first spectral signal processor includes:

i. a transform function operative to transform said first digital output signal from said time domain to said frequency domain, thereby providing a first transformed digital signal;

ii. a spectral analysis unit operative to perform spectral analysis in said frequency domain using said first transformed digital signal and to provide output frequency information that includes a dynamic frequency range divided into above-threshold frequencies and below-threshold frequencies, each said above-threshold frequencies and below-threshold frequencies including respective spectral peaks;

iii. a digital filter operative to filter an output signal received from said ADC1 and to output a filtered signal with strongly attenuated below-threshold frequencies, and

iv. a first digital-to-analog converter (DAC1) operative to convert said output filtered signal into said output analog subtraction signal, and

v. a post DAC filter operative to attenuate said below-threshold frequencies, thereby providing additional improvement of quantization noise and errors of said DAC1.

63. (new) The apparatus of claim 53, wherein said first spectral signal processor includes:

i. a transform function operative to transform said first digital output signal from said time domain to said frequency domain, thereby providing a first transformed digital signal;

ii. a spectral analysis unit operative to perform spectral analysis in said frequency domain using said first transformed digital signal and to provide output

frequency information that includes a dynamic frequency range divided into above-threshold frequencies and below-threshold frequencies;

iii. a digital filtering unit operative to strongly attenuate said below-threshold frequencies and to transfer without attenuation said above-threshold frequencies to provide a digitally filtered output;

iv. a plurality of inverse transform functions operative to inversely transform said digitally filtered output into separate respective inversely transformed outputs; and

v. a subtraction signal synthesizer that synthesizes above-threshold frequency signals from said respective inversely transformed outputs

64. (new) The apparatus of claim 54, further comprising:

f. a calibration/equalization unit operative to calibrate the apparatus.

65. (new) The apparatus of claim 64, further comprising:

g. a signal conditioner operative to condition said secondary subtraction channel analog signal before its input to said ADC2, and

h. a transform function operative to receive said second digital output signal from said ADC2 and to transform said second digital output signal from said time domain to said frequency domain, thereby obtaining a second transformed digital signal in the frequency domain.

66. (new) A method for implementing a high-performance converter comprising the steps of:

a. providing a conversion unit operative to convert an input signal obtained in a time domain, said conversion unit including at least two lower-performance converters, each said converter having at least one lower performance parameter than the high-performance converter;

b. providing a processing unit coupled to said conversion unit and operative to process frequency domain information extracted from said input signal, and, based on said processed frequency domain information, operative to provide in combination with said conversion unit at least two processed signals; and

c. providing a recombining unit operative to combine said at least two processed signals into a single high-performance output signal.

67. (new) The method of claim 66, wherein said input signal is a time domain input signal, wherein said processing of frequency domain information includes:

i. processing a frequency domain signal from said time domain input signal using said at least two lower performance converters by::

A. transforming said time domain input signal into said frequency domain signal in a digital form,

B. dividing said frequency domain into at least two frequency domain parts, a first said part related to a low-resolution signal to noise ratio (SNR) and a second said part related to a high-resolution SNR, thereby extracting said frequency domain information from said frequency domain signal in a digital form, and

C. using said frequency domain information to obtain said at least two processed signals;

and wherein said combining of at least two processed signals into a single high-performance output signal includes recombining said at least two processed signals to obtain a first final output signal from the high-performance converter;

whereby the method provides higher performance and other advantages vs. comparable data conversion methods that work in the time domain.

68. (new) The method of claim 67, wherein said dividing of said frequency domain into at least two frequency domain parts includes providing a threshold above said low-resolution SNR part that determines said division, thereby providing above-threshold frequencies in a window W1 and below-threshold frequencies in a window W2, wherein said W1 and W2 are correlated respectively with said first and seconds frequency domain parts.

69. (new) The method of claim 68, wherein said time domain input signal is an analog signal, wherein said high-performance converter is a high-performance analog-to-digital converter (ADC), wherein a first of said at least two lower performance converters is a first high-speed, low-resolution analog-to-digital converter (ADC1), and wherein said transforming further includes using said ADC1 to convert a subtraction channel representation of said time domain analog input signal into a first time domain digital output signal which is fed to a first spectral processor.

70. (new) The method of claim 69, wherein a second of said at least two lower performance converters is a second analog-to-digital converter (ADC2), wherein said

transforming is preceded by splitting said analog input signal into a main channel signal representation and into said subtraction channel signal representation, both said signals representing said analog input signal, and wherein said processing of frequency domain information further includes:

ii using said first spectral processor to process said first time domain digital output signal and to obtain above-threshold frequency information in a digital form; and

iii. generating, by said first spectral processor and using said above-threshold frequency domain part, a first digitally filtered output signal and an analog subtraction signal, said analog subtraction signal subtracted in a subsequent subtraction operation from said main channel signal, said subtraction operation providing an analog error signal.

71. (new) The method of claim 70, wherein said processing of frequency domain information further includes

iv. processing said analog error signal formed in said subtraction operation,

v. converting said error signal into a second digital output signal using said ADC2,

and wherein said recombining said at least two processed signals to obtain a first final output signal from the high-performance converter includes digitally combining said first digitally filtered output signal and said second digital output signal into a first final digital output signal, using a first digital combining unit.

72. (new) The method of claim 68, wherein said time domain input signal is a digital signal, wherein said high-performance converter is a high-performance digital-to-analog converter (DAC) having both high-resolution and high-speed, wherein a first of said at least two lower performance converters is a DAC with the same high-speed but lower resolution than said high-performance DAC while all the rest of said at least two lower performance DAC are lower-speed, high-resolution DACs, and wherein said transforming includes directly transforming said input signal from said time domain into said frequency domain.

73. (new) The method of claim 72, wherein recombining said at least two processed signals to obtain a final output signal from the high-performance converter includes parallel frequency interleaving of said at least two processed analog signals.

74. (new) The method of claim 68, wherein said recombining said at least two processed signals to obtain a final output signal from the high-performance converter includes obtaining a first final digital output signal in a domain selected from the group consisting of a time domain and a frequency domain.

75. (new) The method of claim 71, further comprising the step of coupling a second spectral processor to said ADC2 and said first digital combining unit to provide at least one additional subtraction stage.

76. (new) The method of claim 71, further comprising the step of combining said first digital output signal from said ADC1 and said second digital output signal from said ADC2 in a second digital combining unit to optionally provide a second final digital output in a time domain.

77. (new) The method of claim 71, wherein said dividing of said frequency domain into at least two frequency domain parts is performed using a spectral analysis unit included in said first spectral processor, wherein said generating of a digitally filtered output signal is performed by a digital filtering unit coupled to said spectral analysis unit and wherein said generating of an analog subtraction signal is performed by a digital-to-analog converter coupled to said digital filtering unit through an inverse transform function.

78. (new) The method of claim 70, wherein said at least two converters are Analog-to-Digital Converters (ADCs) in a subranging/pipeline arrangement, wherein said processing of frequency domain information further includes:

i. converting said analog error signal into a second digital output signal using said ADC2,

ii. transforming said second digital output signal into a second frequency domain signal,

iii. digitally filtering said second digital frequency domain signal by W1 to obtain a second digitally filtered output signal, and

iv. equalizing said second frequency domain signal and subtracting the result of said equalization from said first digitally filtered output signal in said W1 frequency range to obtain an improved resolution first digitally filtered output signal;

and wherein said recombining said at least two processed signals to obtain a first final output signal further includes

v. summing vectorially said improved resolution first digitally filtered output signal and said second digitally filtered output signal to provide a frequency domain digital output signal, thereby obtaining better resolution within a FFT bin.

79. (new) A method for implementing a high-performance data converter comprising the steps of:

a. processing a time domain input signal into a frequency domain signal in a digital form using at least two data converters having each at least one lower performance parameter than the high-performance converter in order to obtain at least two processed signals; and

b. recombining said at least two processed signals to obtain a final output signal from the high-performance converter;

whereby the method provides higher performance and other advantages vs. other data conversion methods.

80. (new) The method of claim 79 wherein said step of processing a time domain input signal into a frequency domain signal in a digital form using at least two data converters includes using at least two analog-to-digital Converters (ADCs) in a filter bank ADC arrangement, each said ADC converter having high resolution,

whereby the method provides increased sampling rate and other advantages vs. other parallel data conversion methods, by combining at least two ADCs in parallel in the digital frequency domain and by use of digital processing in the frequency domain.

81. (new) The method of claim 79 wherein said step of processing a time domain input signal into a frequency domain signal in a digital form using at least two data converters includes using at least two digital-to- analog Converters (DACs) in a filter bank DAC arrangement, each said DAC converter having high resolution,

whereby the method provides increased sampling rate and other advantages vs. other parallel data conversion methods, by combining at least two DACs in parallel in the digital frequency domain, by use of the digital processing in the frequency domain.

82. (new) The method of claim 79, wherein said at least two converters are analog-to-digital converters (ADCs) in a subranging/pipeline arrangement, wherein said step of processing includes:

i. splitting an input analog signal into two signals, one analog signal input to a first ADC (ADC1) to provide a first time domain digital output signal, and the other analog signal input into a subtractor;

ii. transforming said first ADC1 time domain output signal into a first frequency domain signal,

iii. equalizing said first frequency domain signal to obtain a first equalized frequency domain signal,

iv. inverse transforming said first equalized frequency domain signal into a time domain digital signal,

v. creating an analog subtraction signal from said time domain digital signal using a digital to analog converter,

vi. obtaining an error signal by subtracting said analog subtraction signal from said analog signal input into the subtractor,

vii. converting said error signal into a second time domain digital output signal using a second ADC (ADC2),

viii. transforming said second time domain digital output signal into a second frequency domain signal, and

ix. equalizing said second frequency domain signal to obtain a second equalized frequency domain signal and subtracting said second equalized frequency domain signal from said first frequency domain signal,

and wherein said step of recombining includes

x summing vectorially said first equalized time domain signal and said second equalized frequency domain signal to provide a frequency domain digital output signal, and

xi. transforming said frequency domain digital output signal into a time domain signal using an inverse transform to obtain said final output signal.

Respectfully Submitted,

Mark M. Friedman
Attorney for Applicant
Registration No. 33,883

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